AURORA SEMICONDUCTOR

*the **4DHSiP** ™ foundry*

4DHSiP™ (4D Heterogeneous System in Package)

A Disruptive Technology for Advanced Packaging

NASA Electronic Parts and Packaging

June 29, 2017

AURORA SEMICONDUCTOR

Table of Contents

4DHSiP™ = 4D Heterogeneous System in Package

AURORA SEMICONDUCTOR

About Aurora (1/2)

Aurora is an American owned, US-based pure play foundry specializing in multichip module [MCM] packaging:

- Our 4DHSiP™ technology is **patent protected**
- We are a critical manufacturing partner of Draper Laboratory from whom Aurora purchased its St Petersburg facility in January of 2016
- Our facility is Department of Defense cleared
  - **DMEA Trusted Foundry Program: Accredited Supplier**
  - SCIF is fully accredited
- Our business model supports both low rate initial production (LRIP) and volume commercialization
- We deliver solutions through a world-class ecosystem of partners

AURORA SEMICONDUCTOR

About Aurora (2/2)

- 18,000 ft² clean room, 36,000 ft² potential
- Class 1000, 100 & 10 environments

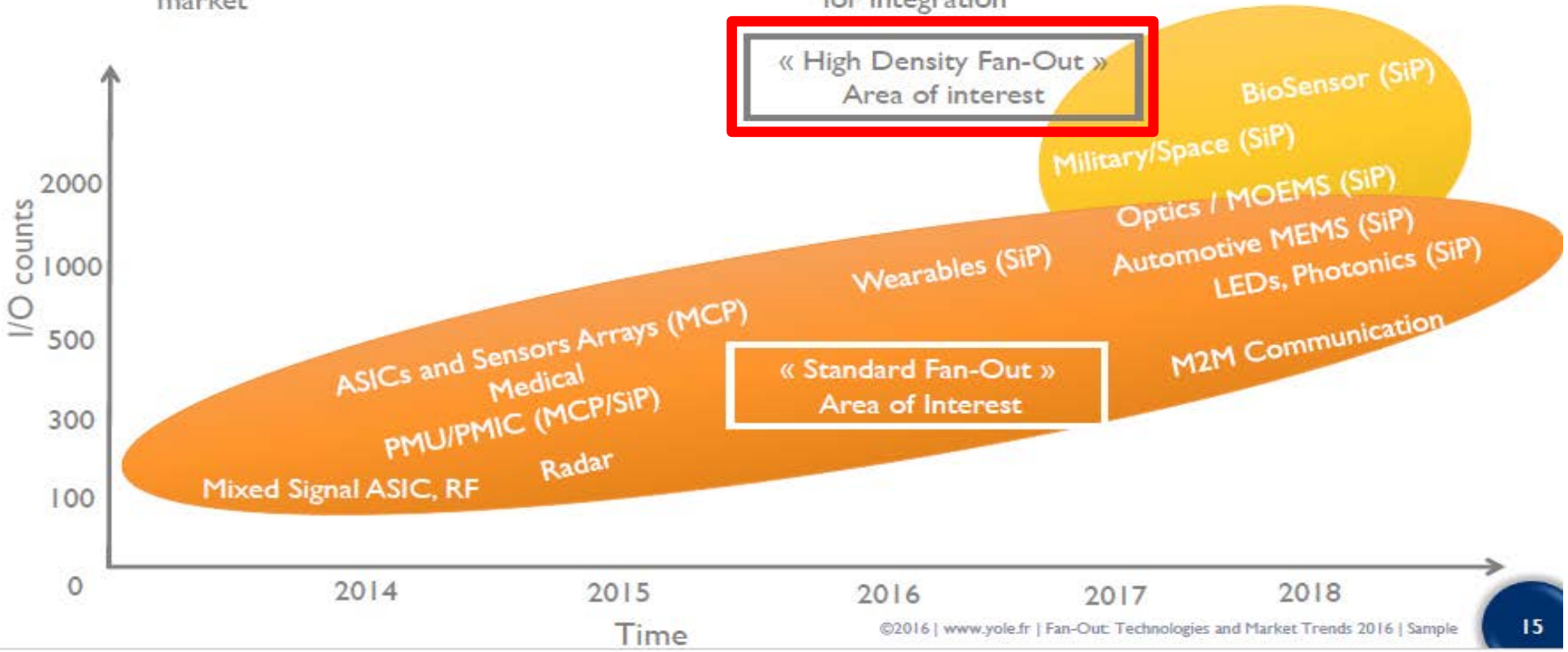
- Secure facility, 24x7 surveillance
- Staffed with cleared employees
- Supported by local universities

TECHNOLOGY ROADMAP FOR FOWLP

Different end-market applications roadmap

Current situation
- « Standard Fan-Out » spreading in automotive and medical apps
- « HD Fan-Out » existing only in Telecom market

Future Fan-Out
- « Standard Fan-Out » spreading to more complex applications to package (MEMS) and SiP
- « HD Fan-Out » to spread thanks to PoP/SiP and needs for integration

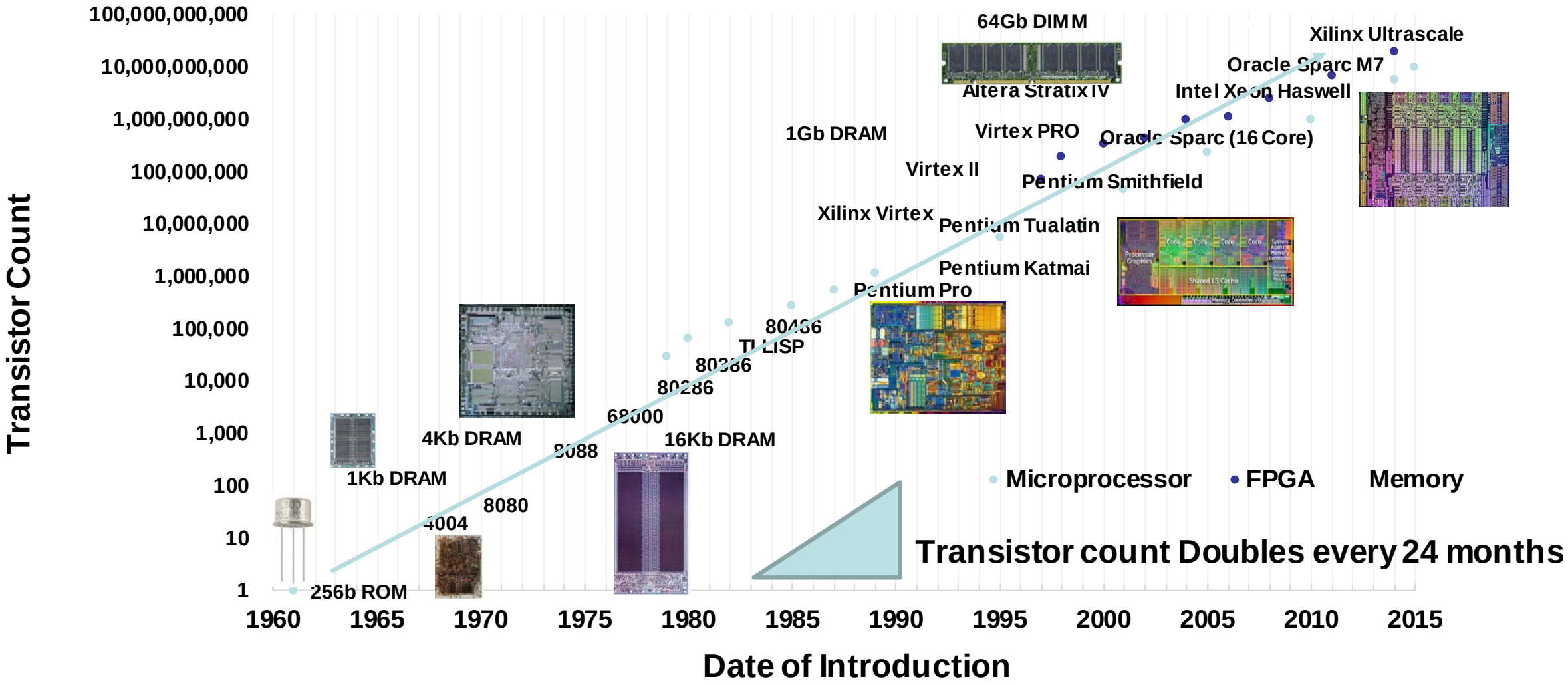


Aurora's 4DHSiP™ Technology

1. Is the most technically advanced – e.g. Amkor, ASE, DECA, TSMC
2. Creates the world's **smallest footprint** & highest interconnect density
   - Up to 100 heterogeneous components in a single multichip module
3. Is capable of innovative **embedded hardware security**
   - Including embedded anti-hacking and anti-reverse engineering
4. Creates the best-in-class performance for complex systems
5. Connects all device technologies – MEMs, sensor, memory, uP, analog, controller etc.; and all substrates – Si, GaAs, InP, etc.
6. Uses TSV (thru substrate via) and *no wire bond or interposer*
7. Stacks **up to 14 interconnect layers**, top and bottom combined
8. Stacks subsystems – i.e. MCMs – up to five high

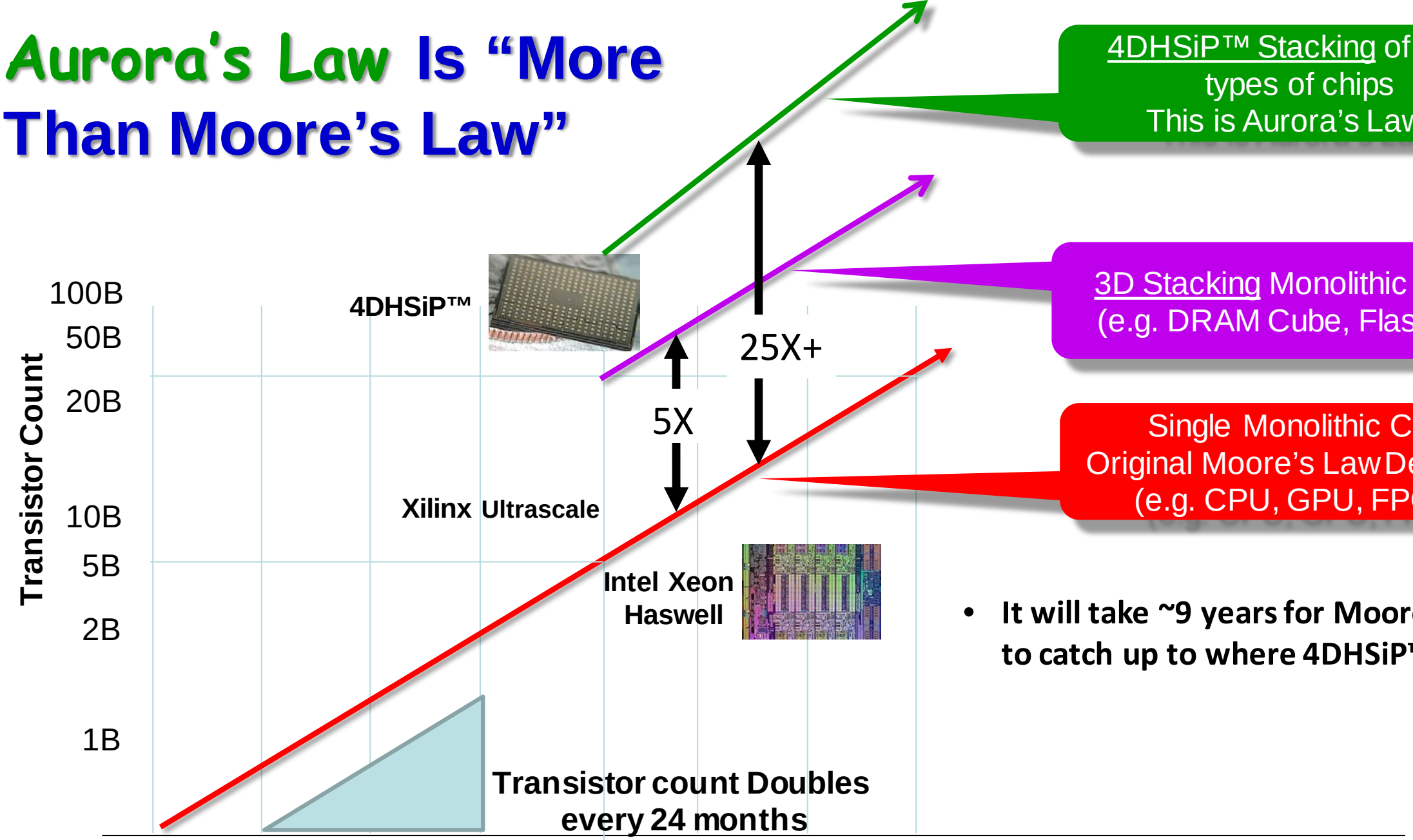
AURORA SEMICONDUCTOR

What Happens to Moore's Law?



AURORA SEMICONDUCTOR

Aurora's Law Is "More Than Moore's Law"

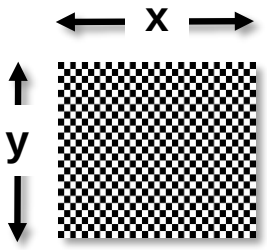


- **It will take ~9 years for Moore's Law to catch up to where 4DHSiP™ is today**

Differentiating Aurora's Law

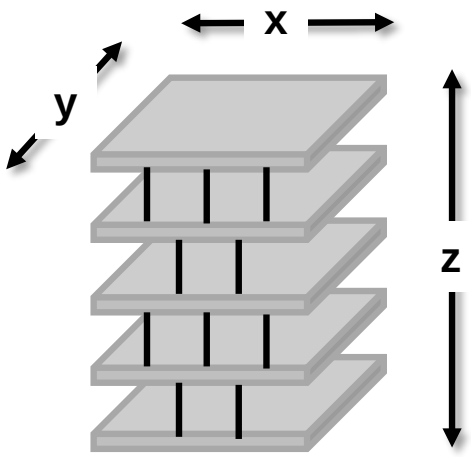
2D
Moore's Law

The number of transistors on an integrated circuit (IC) will double every 18 – 24 months



- It's about **shrinking transistors**
- **2D** = **x** and **y**

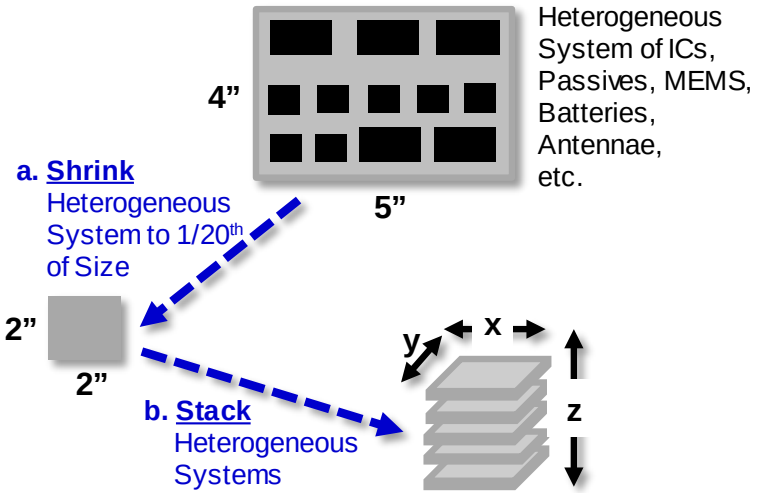
3D
3D Packaging



- It's about **stacking ICs**
- **3D** = **x, y** and **z**

4D
Aurora's Law

Complex systems can be shrunk and stacked using existing technology, creating an enormous density multiplier, at a fraction of the cost



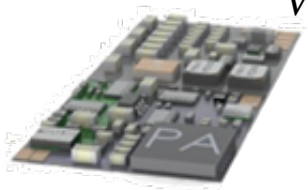
- It's about **shrinking** and **stacking complex electronic systems**
- 5X Stack x 5X Shrink = **25X Density Multiplier**
- The solution when **Moore's Law is technically impracticle** or **too expensive**
- **4D** = **x, y, z** and **Heterogeneous**

AURORA SEMICONDUCTOR

How Do We Do it?

Mix of active & passive IC fab process technologies require hybrid integration

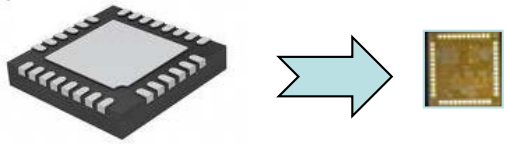
$$\frac{Volume_{TOTAL}}{Volume_{Active}} = 500$$



$$\frac{Volume_{TOTAL}}{Volume_{Active}} = 100$$

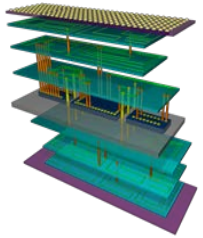
$$\frac{Volume_{TOTAL}}{Volume_{Active}} = 5$$

1st step: eliminate superfluous packaging



2nd step: use chip-scale passives

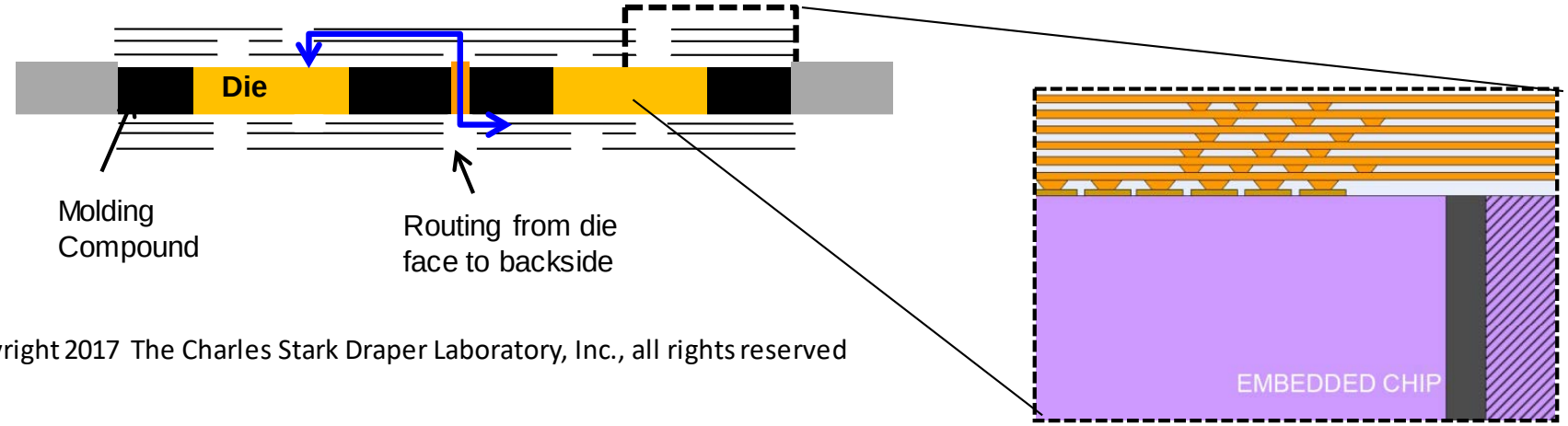
3rd step: μm proximity component integration



AURORA SEMICONDUCTOR

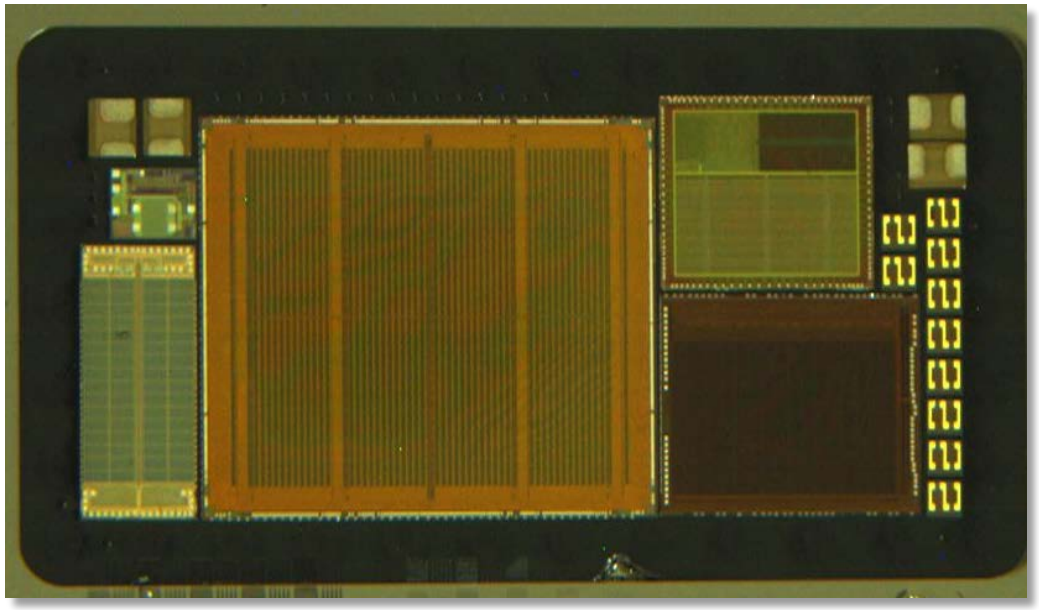
4DHSiP™ Device Features

- Highlight of 4 important features in the figures below
  - All Die (shown as embedded chips) are internally located
    - 4DHSiP™ Benefit: the interconnect layers and surface parts can exist on both sides
  - The die layer forms the substrate upon which succeeding layers are built
    - Results in extremely thin end products (300um to 1200um), which conduct heat readily
  - The die are surrounded by a molding compound
    - This material was chosen for CTE matching and thermal performance
  - Signal conduction through the module occurs on TSV (Thru-Substrate Vias)
    - TSV are chiplets

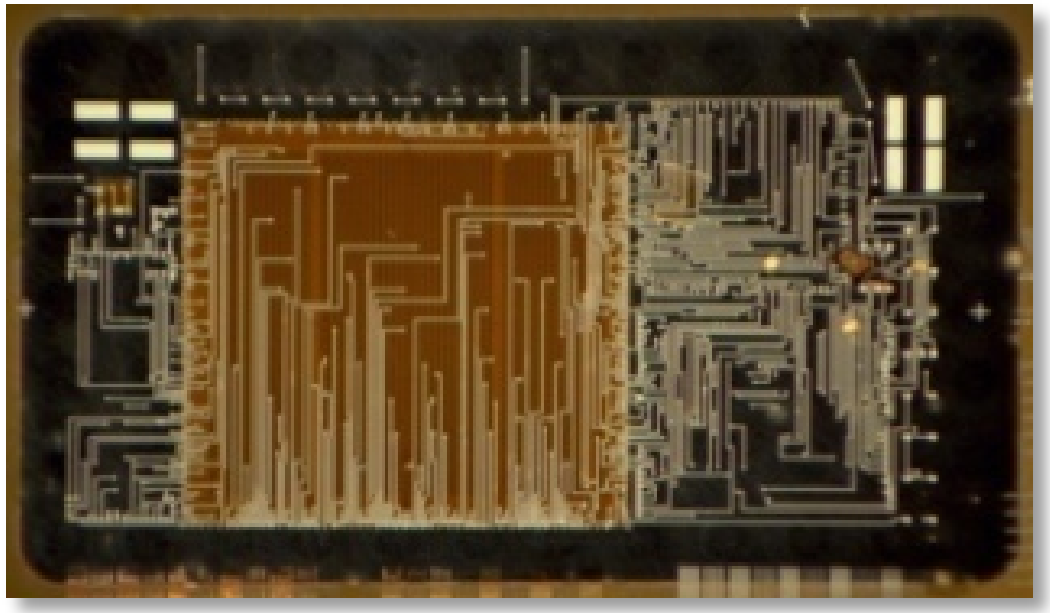


SWaP (Size Weight and Power reduction) with 4DHSiP™

- Reconstituted wafer MCM approach
- Compatible with COTs (commercial off-the-shelf) components
- Leading edge “chips first” technology; FOWLP (Fan Out Wafer Level Package)



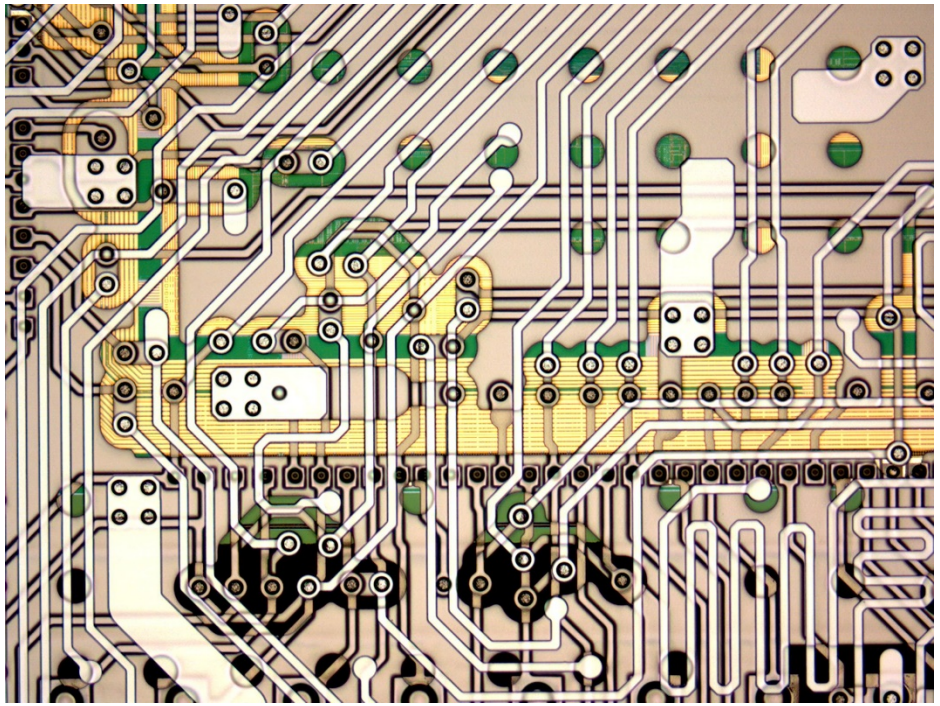
Multi-chip Module
Bare Die, Pre-Interconnect

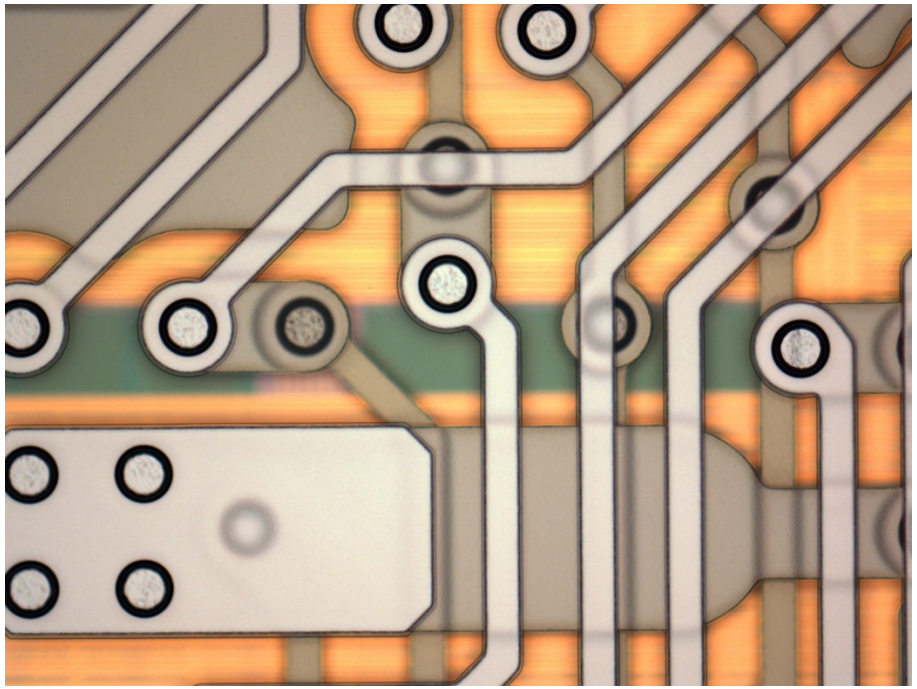


Multi-chip Module
Post-Interconnect

AURORA SEMICONDUCTOR

4DHSiP™ Interconnect Fabric

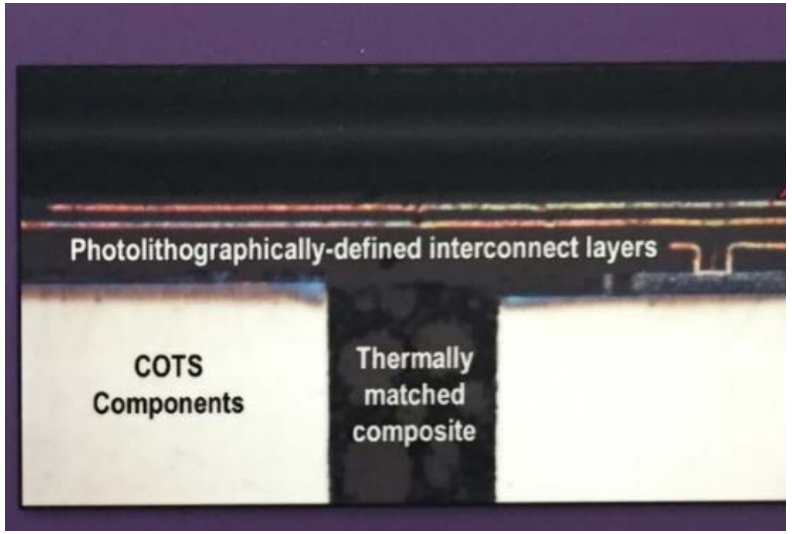


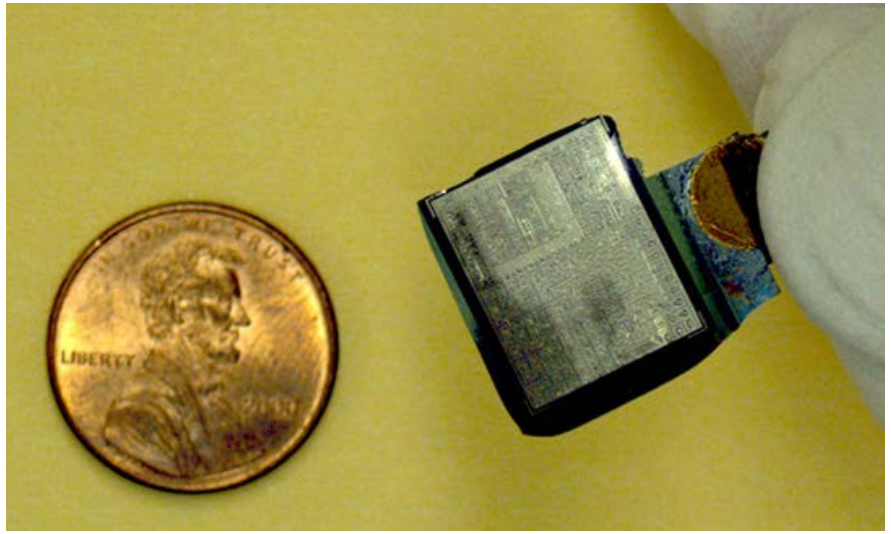


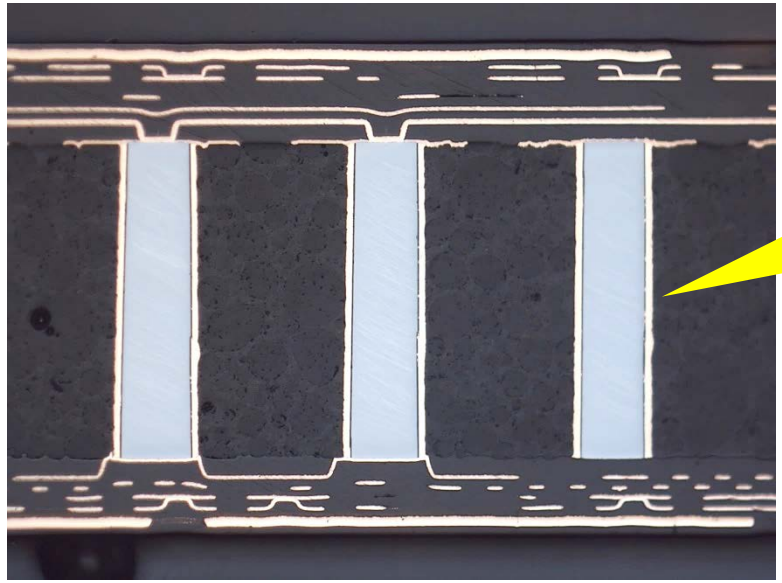
Consider the design possibilities with this interconnect fabric?

- 14 total layers of interconnect (7 topside and 7 bottom)
- Controlled Impedance Transmission lines and Differential Pairs
- Power/Gnd Bus; Multiple Power Domains
- Signal line Shielding for crosstalk isolation (Faraday Cage)

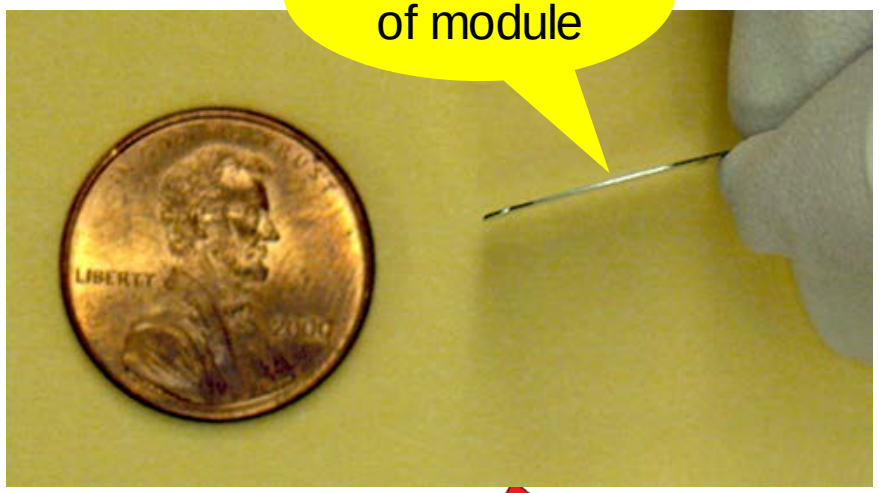
4DHSiP™ = Smallest footprint





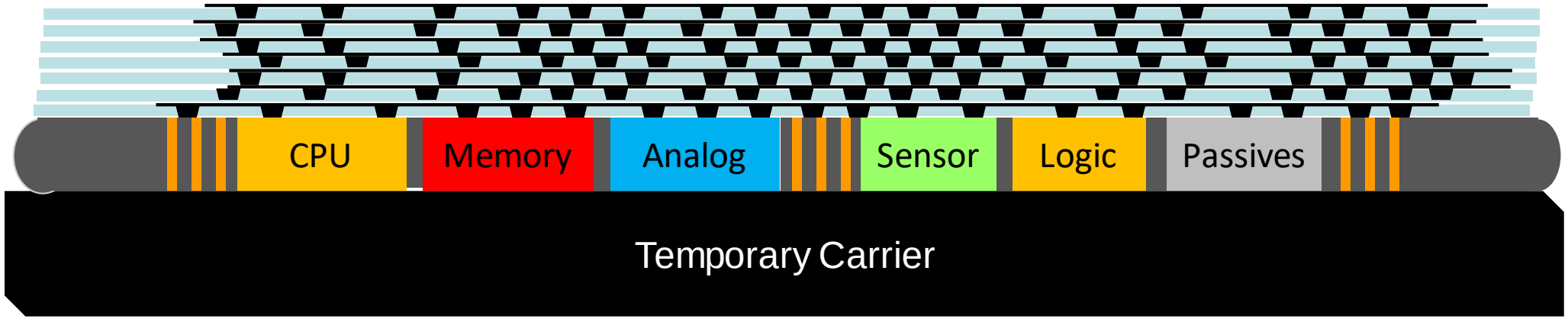


SEM of TSV



Thickness of module

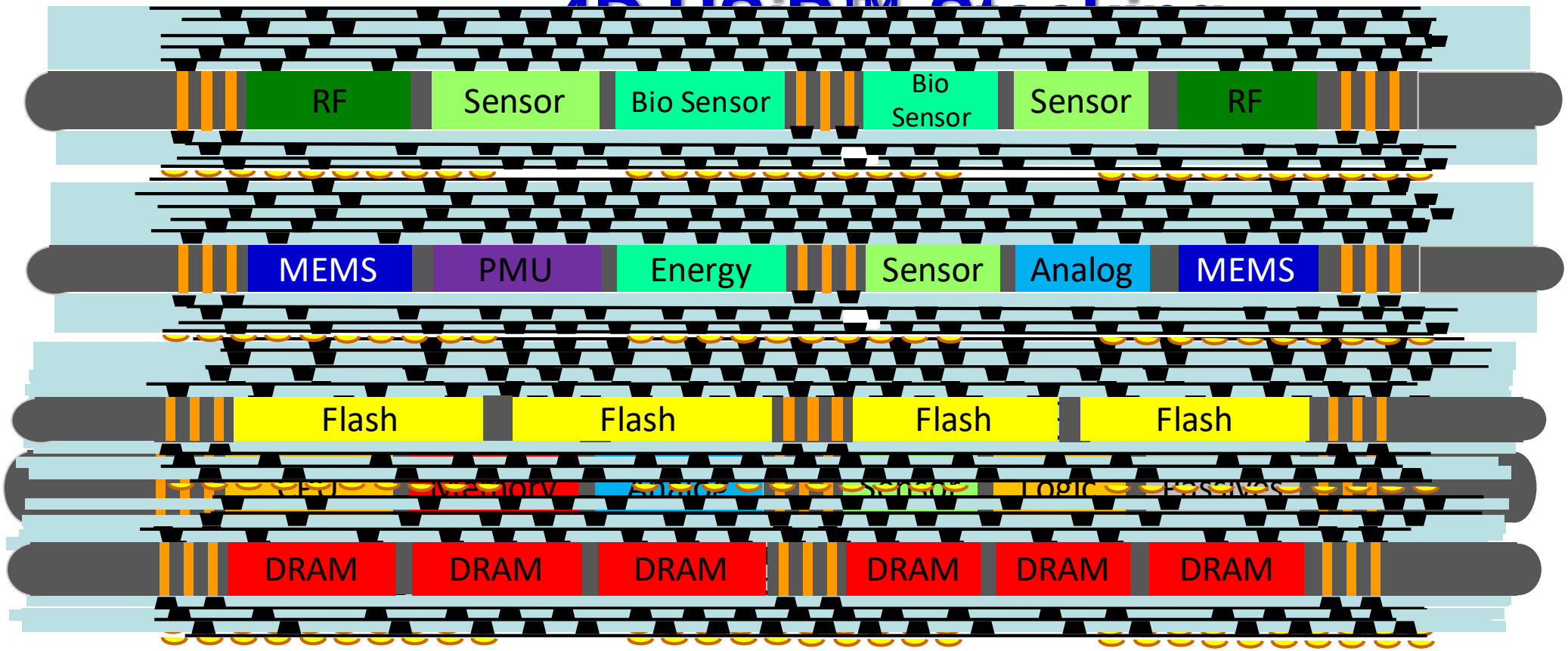
4DHSiP™ Module Construction



Top Interconnect Layer 7
Top Interconnect Layer 6
Top Interconnect Layer 5
Top Interconnect Layer 4
Top Interconnect Layer 3
Top Interconnect Layer 2
Top Interconnect Layer 1
Via Contact to IC pads
First Dielectric Layer
Molding Compound
Through Substrate Via
Heterogeneous IC
Bottom Interconnect Layer 1
Bottom Interconnect Layer 2
Bottom Interconnect Layer 3
Bottom Interconnect Layer 4
Bottom Interconnect Layer 5
Bottom Interconnect Layer 6
Bottom Interconnect Layer 7
BGA Bumps

AURORA SEMICONDUCTOR

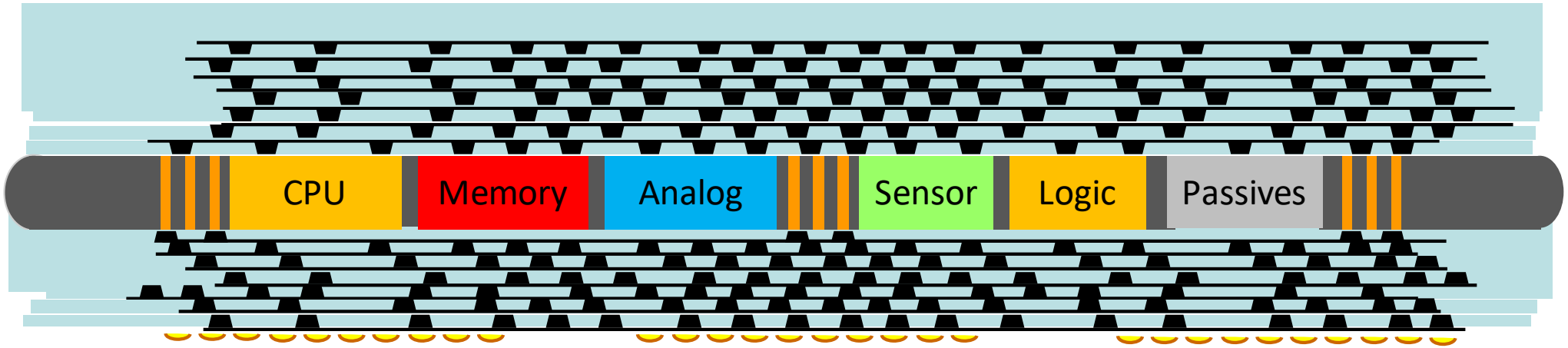
4D HSiP™ Stacking



HSiP Layer	# Metal Layers	Cum. # IC & Passives	Thick-ness (µm)
5	70	500	1300
4	56	400	1050
3	42	300	800
2	28	200	550
1	14	100	300

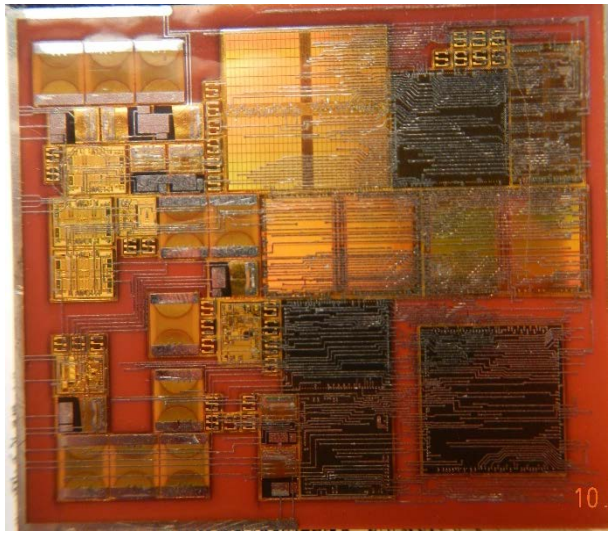
AURORA SEMICONDUCTOR

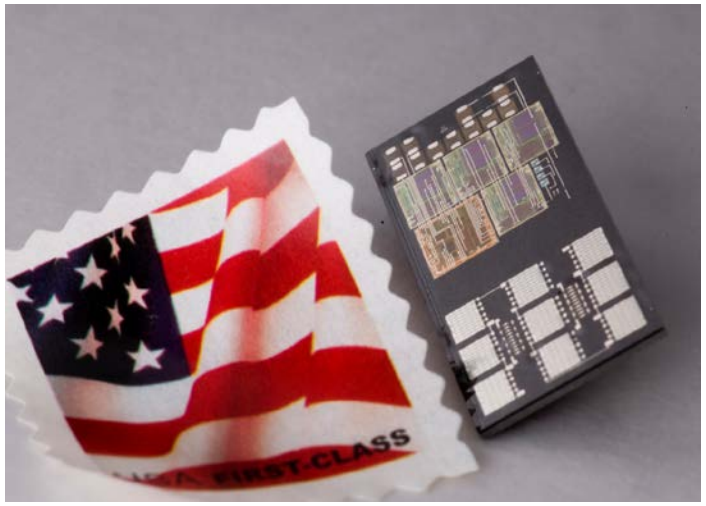
Integrated Hardware Security



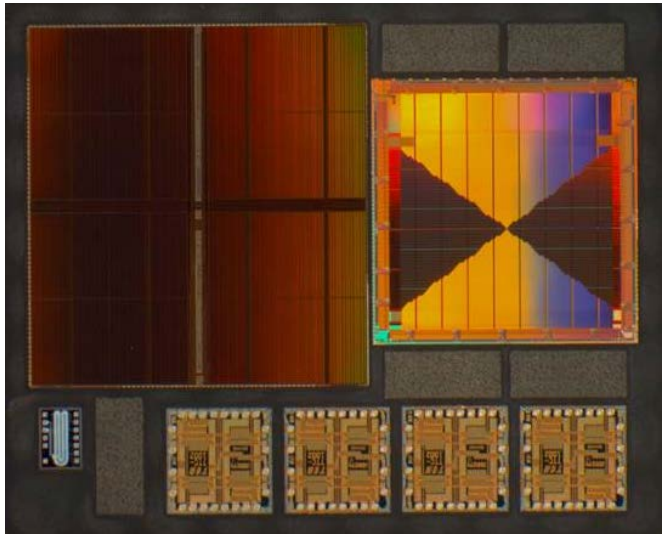
- **4DHSiP™ enables our clients to protect their systems with embedded hardware security for anti-hacking as well as anti-reverse engineering**
  - Interconnect or via layers can be individually personalized for each HSiP™ module with an encoded key to create an non-erasable, **anti-hacking defense**
  - Interconnect layers may be designed as obfuscation layers – i.e. series of mazes, dead ends and booby traps – that protect against **reverse engineering**
- These hardware security enhancements will empower system designers in every market segment

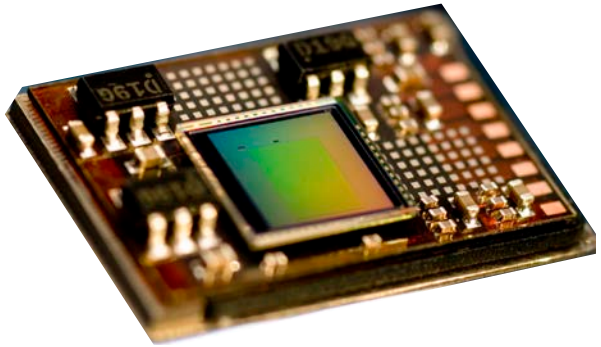
Miniature Electronic Systems Examples



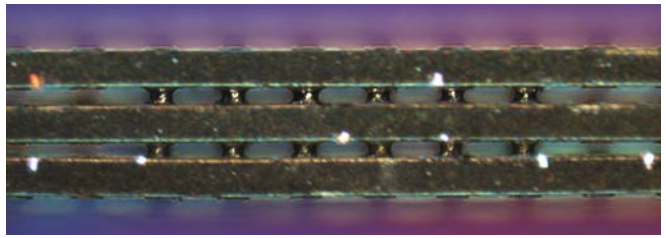


Without surface mount parts

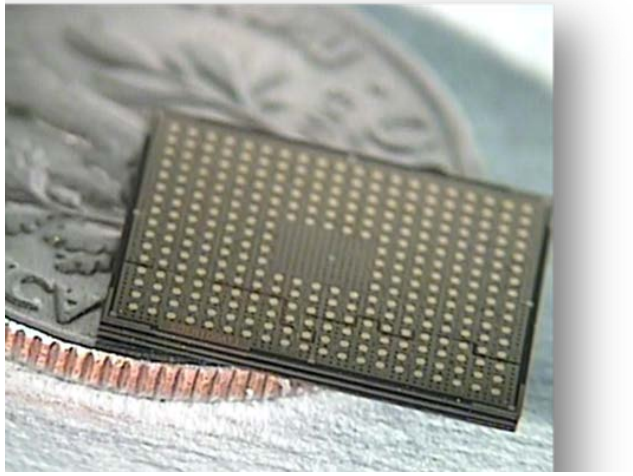




With surface mount parts

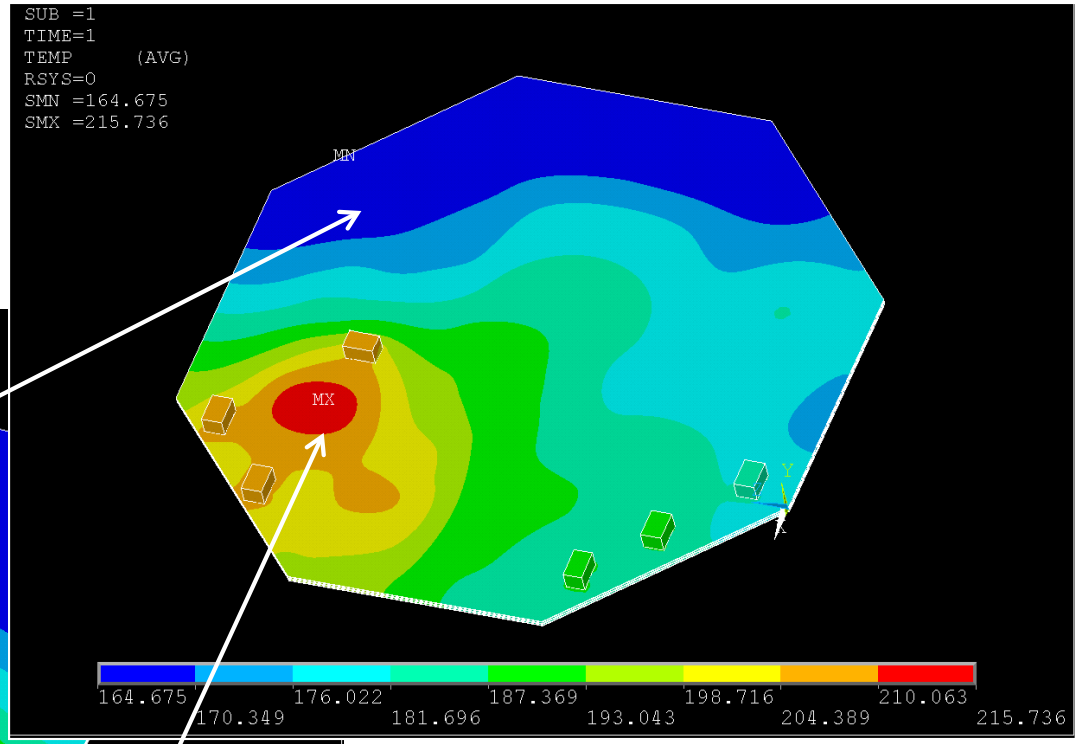


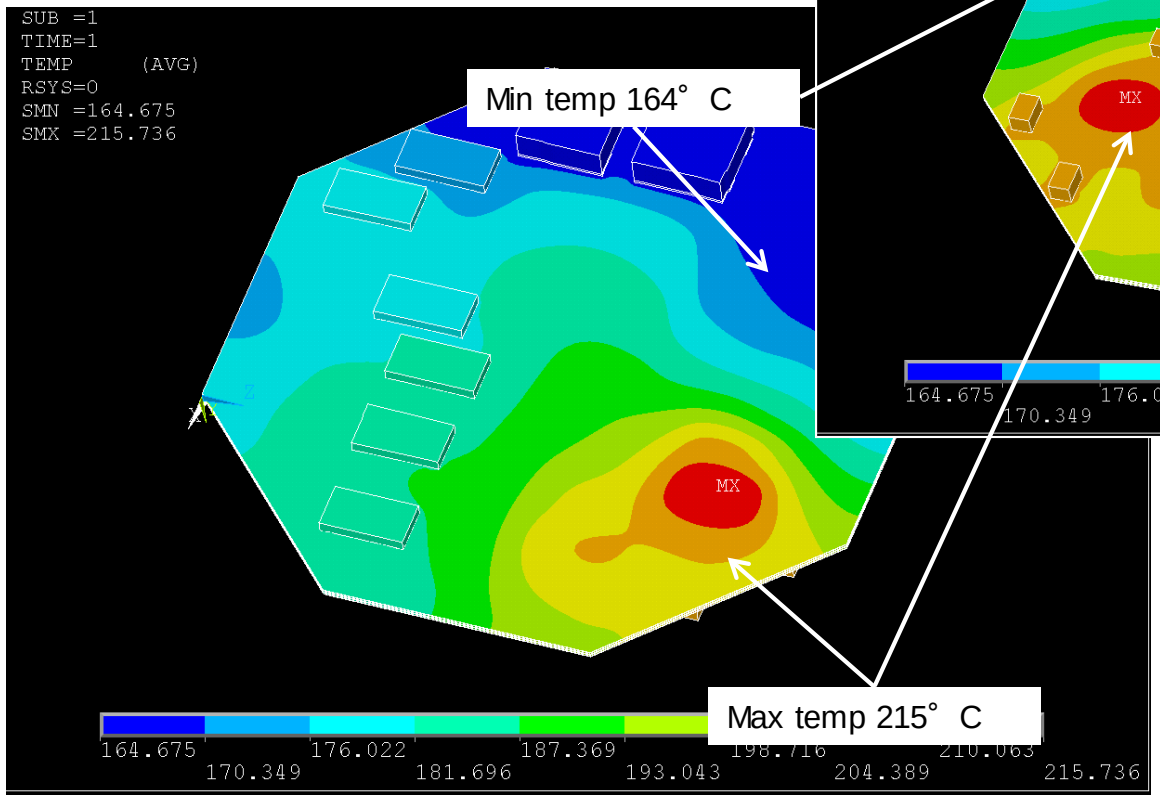
Stacked Module



Thermal FE Analysis
3D Baseline Temperature Contour Top and Bottom

Top



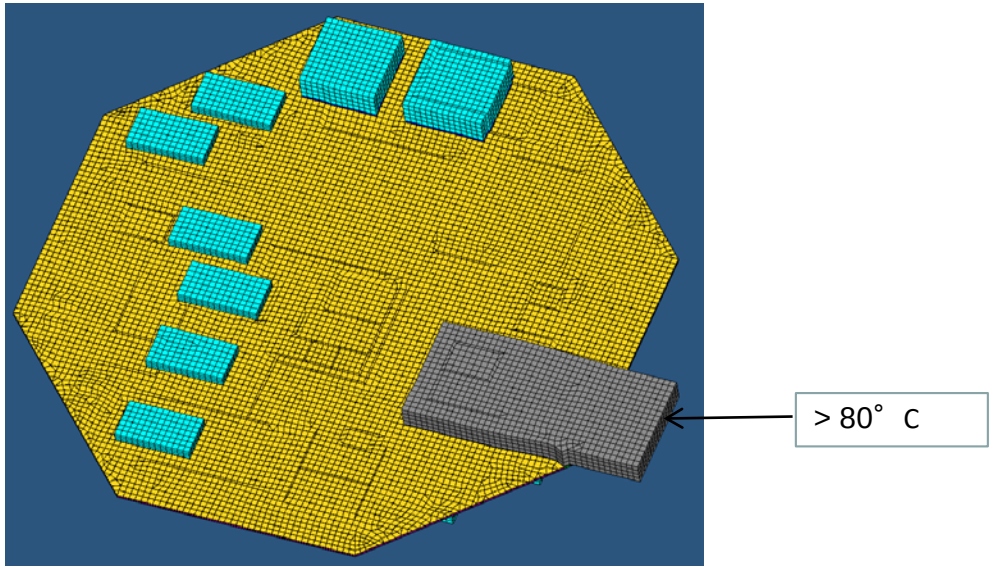


Bottom

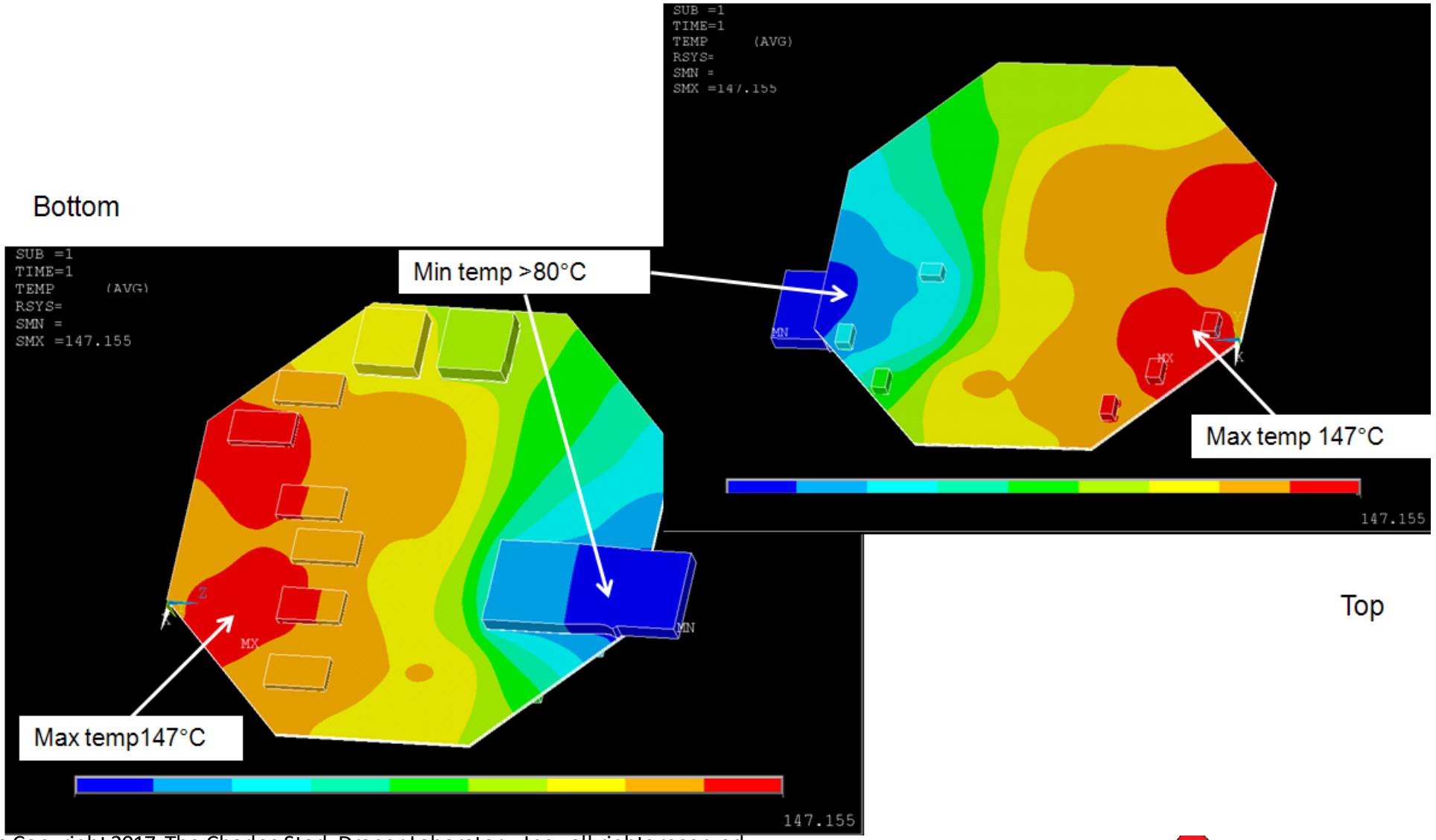
AURORA SEMICONDUCTOR

Adding a Thermal Bridge

- Thermal bridge added to shunt heat from the surface of the module to the housing
  - Devised as an aluminum block 2mm thick
  - Added 50µm of Zymet thermal compound to adhere bridge to the surface
  - Sized to cover the area permeated with thermal fins for maximum heat transfer
  - Set a boundary condition for the housing contact surface
    - In both single and 3D stacks set the temperature to greater than 80° C



3D Stack with Thermal Bridge
Steady State Temperature Contour Top and Bottom



AURORA SEMICONDUCTOR

4DHSiP Reliability

Over the past 8 years thousands of 4DHSiP modules have been shipped for classified projects with zero returns for reliability reasons.

Testing done by Draper and the customers have met program reliability requirements:

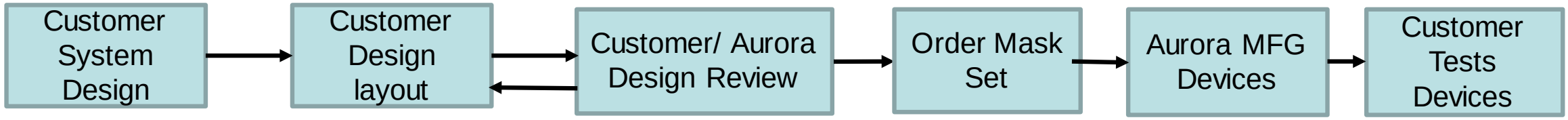
- HTOL – 1000 hrs 125C – Pass
- Temperature cycle – 2000 cycles -29C to 85C – Pass
- THB 1000 hours 85C 85% humidity – Pass

Additional testing has been done with no failures but needs to be declassified.

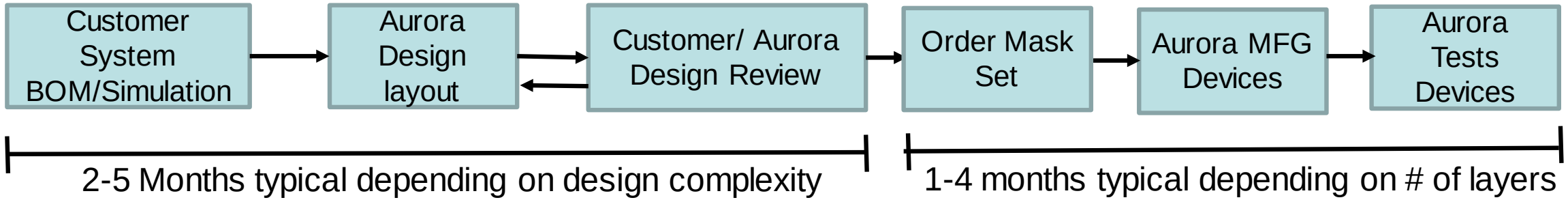
Engagement Options

Two primary engagement options are available today. Both use verified Aurora Design rules and DRC Rules.

Customer does Design - Aurora does Manufacture



Aurora does Design and Manufacture



Aurora suggests an Initial phase through design verification or initial samples to allow customers to get comfortable with the 4DHSiP process and results

AURORA SEMICONDUCTOR

Protected-Classified 4DHSiP™ Ecosystem

Customer or Aurora
Material
Procurement

INTEGRA TECHNOLOGIES

Testing & Analytical

AURORA SEMICONDUCTOR

4DHSiP™ Manufacturing

DRAPER

Or Customer

R&D & Design

AURORA SEMICONDUCTOR

Non Classified 4DHSiP™ Ecosystem

Customer or Aurora Material Procurement

INTEGRA TECHNOLOGIES

Testing & Analytical

AURORA SEMICONDUCTOR

4DHSiP™ Manufacturing

treehouse
your solutions portal

Or Customer Design

bridg
Bridging the Innovation Development Gap

Research & Development

AURORA SEMICONDUCTOR

Summary 4DHSiP™ – A Disruptive Technology

4DHSIP™ is an excellent solution for low to medium volumes and some high volume applications

- Systems with multiple die types at different silicon nodes or heterogeneous wafer processes
- OEM's who want to increase functional performance and stay at current wafer nodes
- System customers who need performance, size and weight advantages on existing designs
- Customers who want hardware security built into the system at a reasonable cost

Show us your system problem and allow Aurora to analyze your design needs and propose a solution

- Take your existing or new design requirements and volumes and Aurora will propose a physical design solution with estimated costs (Analysis with hardware security is available)
- Do your own analysis with our design rules and we can estimate the cost at target volumes
- Run a demonstration project to show what 4DHSiP™ can do for your design in terms of performance, reliability and security (if required)

One Last Thing

Aurora Selected for Air Force SBIR AF171-121 Award

This project will demonstrate the feasibility of building complex multichip modules (MCMs) with Aurora Semiconductor's 4DHSiP™ process from integrated circuit die harvested using Aurora's BondCoin™ DER technology.

Thank You

Bruce Barbara– Director of Technical Marketing
bruce.barbara@aurorasemi.com

Links

- Aurora: www.aurorasemi.com
- Draper: www.draper.com
- Bridg: www.gobridg.com
- Integra: www.integra-tech.com
- Treehouse: www.treehousedes.com